Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

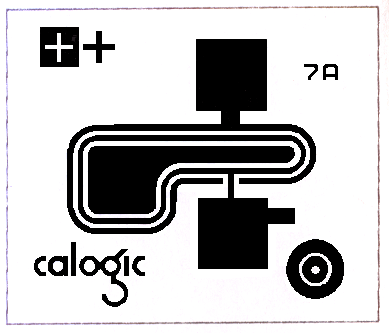
**S SOURCE**

**D DRAIN**

**G GATE**

**.023”**

**.021”**



**DIE ID**

**SD210**

**S**

**D**

**G**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: SD210**

**APPROVED BY:DK DIE SIZE .021” X .023” DATE: 2/7/17**

**MFG: CALOGIC THICKNESS: .008” P/N:SD210**

**DG 10.1.2**

#### Rev B, 7/19/02